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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/976,641
Filing Date: October 12, 2001
Appellant(s): XU ET AL.

Timothy Trop
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/30/2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is substantially correct. The following comments are added to assist the Board in better understanding the present appeal.

Just like the present invention, Ovshinsky also discloses a memory cell array, each cell comprising a phase change material formed over an underlying pn diode wherein the n+ region of the pn diode is: (1) subjacent the p-type region of the pn diode; (2) is formed in a p-type substrate; and (3) serves as the wordline. From a physics-concepts standpoint, the only significant difference between the present invention and Ovshinsky's is that the present invention's pn diode further includes an additional n-type region that is subjacent the n+ wordline and which separates this wordline from the oppositely-doped p-type substrate to reduce substrate leakage currents. Chang teaches this element missing from Ovshinsky, and provides

motivation as to why the skilled artisan would have been motivated to add it to Ovshinsky. In fact, the issue—whether one would have **desired** to add this further n-type region between Ovshinsky's n+ channel/wordline 12 and p substrate—is **not** disputed by Appellant, nor raised on appeal.

The rest of the differences, as claimed, between the present invention and Ovshinsky relate to minor, conventional semiconductor processing issues. Most of these minor processing issues are not relevant to this appeal either. Rather, the present appeal relates only to whether forming all four of the n/n+/n/p diode layers *solely in bulk Si* was an obvious alternative to forming some of the upper layers in an additional Si region epitaxially-grown on the Si substrate (an epi-Si region), and whether the prior art reasonably teaches or suggests that this conventional modification was possible.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 11-14 and 16-30 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5359,205	OVSHINSKY	10-1994

6,015,995	CHANG	1-2000
5,502,326	SLOTBOOM et al.	3-1996
4,599,705	HOLMBERG et al.	7-1986

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 11, 12 and 16-30 are rejected under 35 U.S.C. l03(a) as being unpatentable over Ovshinsky '205 in view of Chang '995 and Slotboom et al. '326.

a. Ovshinsky discloses a memory storage array employing phase-change memory material and includes the following structures (see e.g., FIG. 1 and cols. 15-16): a p-type semiconductor substrate 10 (unnumbered in FIG 1); a plurality of buried n+ channels (wordlines) 12 that couple various memory cells (see e.g., FIG 3); an n epitaxial layer 14; isolation trenches 16 on either side of each of the buried lines 12; p+ diffusion layer 24; SiO2 insulation layer 20 having a plurality of apertures (or pores) 22; metal contact 32; memory material 36 having a lower portion which extends into the insulation pores 22; and upper contact 40. Restated, Ovshinsky discloses all of the limitations of the listed claims except for (1) the presence of a lightly doped n-type region interposed between the n+ wordline 12 and the p-type substrate, and (2) the limitation that the diode structure may be formed in a bulk substrate as opposed to a bulk/epi substrate.

b. Chang is directed towards a ROM diode array having n+ conductive lines 32 diffused into a p-type bulk substrate 20 with a p+ regions 40 diffused, in turn, into the n+ conductive lines 32 to form the memory diode. Chang further teaches that additional, more lightly doped n-diffusion regions 38 are formed under the n+ conductive lines 32, all in the bulk Si substrate, for

the purpose of preventing current leakage between the n+ conductive lines 32 and the p-substrate 20 (e.g., col. 4, lines 10-). It would have been obvious to one of ordinary skill in the art at the time of the invention to have further included additional, more lightly doped n-type regions between the n+ channel and p-substrate of the Ovshinsky memory device for the purpose of reducing current leakage as taught by Chang.

c. The previously added language to the independent claims sets forth that the substrate is a bulk substrate, thus distinguishing the structure from a pn diode that is formed in/on a bulk substrate as well as an epitaxial layer formed on the bulk substrate, as taught by Ovshinsky. Chang teaches that pn diodes can alternatively be formed exclusively in bulk substrates without the inclusion of an epi layer, as opposed to being formed in the combination of bulk regions and overlying epi regions of a substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to have formed all of the pn diode's bulk and epi regions as taught by Ovshinsky/Chang solely in a bulk substrate without growing an epilayer, as taught by Chang for the purpose of simplifying the manufacturing process and thereby reducing the associated manufacturing costs.

d. The independent claims have also been amended to further recite that a pair of trenches are disposed on either side of the buried line and extend past "said buried line and said region of a second conductivity type into said substrate under said buried line." Ovshinsky and Chang both teach oxide isolation regions (16 and LOCOS isolation 30, respectively) for isolating the diodes, but neither reference teaches that the isolation structure extends below the buried line.

i. Slotboom teaches pn junction diode memory structures comprising (see e.g., FIG 2a) within a type 11 substrate 1, a plurality of: a type I region 4 and type II layer 26 forming a pn

junction 8 that are isolated by SiOx trench isolation structure 27, and a buried type I contact layer 3 for making contact to the lower side 4 of the pn junction. (While FIG 2a depicts the type II substrate being specifically n type, Slotboom further states that all of the conductivity types may be respectively reversed; col. 10, lines 26- .) The SiOx trench isolation structure extends below the buried line 3 and the second conductivity semicircular region of 26 that is adjacent to the pn junction 8, into the substrate. Slotboom teaches that the SiOx isolation structure may be formed either by a LOCOS method (FIG 1) or alternatively by a trench isolation method (FIG 2), and that the trench isolation embodiment possesses various advantages over LOCOS including a greater reduction in lateral size scale (e.g., col. 7, lines 28-) and elimination of an alignment step (col. 7, lines 15-). The depth of the isolation grooves 27 is more than 1 micron so that the length of the current path between adjoining cells is sufficiently great for avoiding breakdown between adjoining cells in spite of the small groove width (col. 7, lines 40-43).

ii. It would have been obvious to one of ordinary skill in the art at the time of the invention practicing a memory device according to Ovshinsky/Chang to have specifically substituted a trench isolation structure as taught by Slotboom for the LOCOS isolation structure of Chen for the reasons cited in Slotboom and restated hereinabove. It would have further been obvious to one skilled the art to have formed this trench isolation structure so as to specifically extend below the buried line of the pn diode into the substrate for the purpose of avoiding breakdown between adjoining cells in spite of the small groove width as taught by Slotboom.

e. Claim 20 further recites that the pore is lined with a sidewall spacer. The Examiner notes that under the broadest reasonable interpretation, the term “sidewall spacer" relates to the method by which the insulation layer and aperture is formed, and nothing in the claim precludes the

sidewall spacer from being formed of the same material as that of the insulating layer. As such, because SiO2 is an amorphous material with no long-range grain boundaries, there is no structural distinction between calling the entire SiO2 layer an insulation layer, or alternatively labeling a portion of the SiO2 as an insulation layer and another portion as a sidewall spacer. Restated, as the portion of SiO2 adjacent the pore forms a sidewall and spaces the pore and its contents from the rest of the insulation layer 20, this adjacent portion can be labeled a sidewall spacer, so the Ovshinsky reference also teaches the language of this claim.

f. Regarding claim 23, in that Ovshinsky is directed towards a digital memory array, and such arrays' primary (if not only) intended use is for storing electronic data in a machine that manipulates digital data (i.e., a computer), it would have been obvious to one of ordinary skill in the art at the time of the invention that the Ovshinsky memory device may be used in a computer for the purpose of using it for its intended purpose, regardless of whether Ovshinsky expressly, implicitly or inherently teaches as much.

g. Regarding claim 24, Ovshinsky further discloses (see e.g., FIG 4 and col. 19) an addressing matrix (interface) 52 and integrated circuitry connections (bus) 53 coupled to the storage array 51. Further, regardless of whether Ovshinsky expressly discusses the presence of a processor, one would inherently be present in the computer and coupled to the storage so that the storage will work for its intended purpose of storing memory that is to be processed by a processor.

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinsky/Chang/Slotboom as applied to claim 12 above, and further in view of Holmberg et al.

'705. As explained above Ovshinsky/Chang/Slotboom teaches all of the limitations of claim 12 and also those limitations set forth in claim 14, but does not teach that the contact is formed under the dielectric layer as recited in claim 13. Rather, Ovshinsky teaches that metal contact 32 is formed in and over the dielectric pore and layer.

a. Holmberg et al. '705 is directed towards a programmable memory array having buried n+ wordline 56 formed on a p-type substrate 54 under n-type region 64 with a chalcogenide phase-change based memory structure formed thereover. The lower platinum silicide memory electrode 60 is formed under the insulation layer 66 and aligned with the insulation pore. It would have been obvious to one of ordinary skill in the art at the time of the invention to have employed the electrode-under insulation structure as taught by Holmberg in the memory device of Ovshinsky at least for the purpose of not taking up addition space in the insulation pore, thereby enabling the pore to be formed of a smaller diameter and, in turn, enabling further miniaturization of the memory array.

b. Regarding claim 14, regardless of whether either of Ovshinsky or Holmberg expressly state that the function of the upper more lightly doped n-region (e.g., Ovshinsky's n epi region 14) is to reduce the reverse bias leakage of the n+ line, the underlying physics of carrier behavior in doped semiconductor junctions dictates that this function will necessarily result due to the presence of the lightly doped n-type layer.

(11) Response to Argument

The present appeal relates only to whether forming all four, n/n+/n/p, diode layers *solely in a bulk Si substrate* was an obvious alternative to forming some of these diode layers in an

additional Si region that is epitaxially-grown on the bulk Si substrate (an epi-Si region), and whether the prior art reasonably teaches or suggests that this conventional modification was, in fact, possible.

More specifically, claim 11 sets forth insulation-trench-isolated diodes formed in a Si substrate. From bottom up, each diode structure is: n-type region 22c (hereinafter, the "1st layer")/n+ region 22b (or "2nd layer")/n-type region 22a (or "3rd layer")/p-type region 20 (or "4th layer"), thereby forming a pn diode in the surface of a p substrate.[1] (see e.g., FIG 1 of the present application). In the preceding Office actions, the examiner readily acknowledged that Ovshinsky does not disclose the further inclusion of a relatively lighter doped n-region (or 1st layer) sandwiched below the n+ wordline (or 2nd layer) and above the p type substrate; the examiner combined Chang for the teaching that it was known to provide such a region. The stated motivation to combine was for the purpose of reducing current leakage into the substrate. This motivation—which is the same reason Appellant employs this lowermost n-type region—was taught by Chang (e.g., col. 4, lines 10-). The claims were further amended during the course of prosecution to further limit the insulating trench structures that isolate the substrate pn diodes. This limitation was further addressed by the combination of the Slotboom isolation structure, wherein trench isolation is employed to isolate pn diodes. Slotboom additionally teaches pn diodes layers (which correspond to the 2nd 3rd and 4th layers) that are formed entirely within the bulk-Si substrate.

Appellant does **not** dispute on appeal (1) whether this combination would have resulted in the same ordering of n and p diode layers set forth in the claims (aside from the question of

whether they are formed in epi-Si vs. bulk-Si); nor (2) whether the skilled artisan would have *desired* to add this further n-type region under the wordline. Rather, Applicant argues (1) that while the combination of Ovshinsky and Chang teaches the 1st through 4th diode layers, neither Ovshinsky nor Chang teaches the top two (3rd n- and 4th p-) diode layers being formed in the bulk Si substrate; and (2) that none of the prior art references teach all four, n/n+/n/p, diode layers being formed in the bulk Si substrate.

The examiner agrees that Ovshinsky does not teach these limitations. That is one of the reasons why the claims were rejected as being obvious over Ovshinsky instead of as being anticipated by Ovshinsky. The examiner also agrees that neither Chang, nor any prior art reference, *when viewed alone*, teaches all four layers of the diode. But these were never the examiner's positions.

Rather, the examiner's position is that Ovshinsky/Chang teaches all four diode layers, albeit formed in a combination of the bulk-Si and epi-Si substrate layers. The examiner additionally stated, though, that it would have been further obvious to have alternatively formed all four of these layers solely in a bulk-Si substrate because this was a conventional, functionally equivalent way of forming doped layers on the surface of a Si substrate. Specifically, both of these two conventional, functionally equivalent alternatives had well-known associated advantages and disadvantages: epitaxially-grown Si (epi-Si) layers were typically of higher crystalline quality than were bulk Si substrates; and as such, the formation of devices, or portions thereof, in epi-Si commonly led to higher quality (e.g., faster) devices. However, epi-Si was more expensive to produce than was a bulk Si substrate. Thus, the particular one of these two

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[1] "N-type" and "p-type" are being used herein for the claim's recitations of "first conductivity type" and "second

conventional options ultimately selected for a given application depended only upon the balancing of the associated conventional considerations, such as the desired device quality and the associated manufacturing costs. The examiner's position—that this difference was obvious because the two structures were functionally equivalent alternatives—was explained in the preceding Office actions.

The examiner's position that formation of all of the diode layers particularly in bulk-Si was a conventional alternative is evidenced by Chang wherein the entire diode—comprised of n region 38/n+ region 32 and p region 40 (corresponding to the 1st, 2nd and 4th diode layers claimed)—is formed entirely within the bulk substrate. This position is further evidenced by Slotboom wherein the entire diode—comprised of n+ region 3/n-region 4 and p region 8 (corresponding to the 2nd, 3rd and 4th diode layers claimed)—is formed entirely within the bulk substrate. [2]

As such, Chang teaches and provides motivation for why one would have wanted to additionally include an n-layer (the 1st layer) under the n+ wordline (2nd diode layer). Chang also provides evidence that it was known *how* to provide an n/n+/p diode structure fully within the bulk substrate (i.e., that it was known how to provide the 1st more lightly doped n layer *under* the 2nd more heavily doped n+ layer, all solely within the bulk substrate). Slotboom provides evidence that it was known how to provide an n+/n/p diode structure fully within the bulk substrate (i.e., that it was known how to provide the 3rd more lightly doped n layer *above* the 2nd more heavily doped n+ layer, all solely within the bulk substrate).

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conductivity type" for brevity and clarity, but in fact, the claim would read on a structure wherein the dopant conductivity types are reversed.

[2] Slotboom's description of FIGs 2a/b alternatively sets forth the conductivity types in the reverse order, i.e., the p+/p/n order, but Slotboom expressly states that the conduction types may be reversed (col. 10, lines 26-).

To summarize, the rejection set forth reasons for why the ordinarily skilled artisan would have wanted to provide the diode with all four of the prior art's, n/n+/n/p, layers. The rejection also set forth reasons why the skilled artisan would have wanted to provide all four of these layers specifically in the bulk substrate region, as opposed to being provided in the combination of the bulk- and epi- substrate regions. Moreover, the rejection provided more than ample evidence that it was known *how* to provide all four of these layers in the bulk substrate region. As such, the examiner has established a *prima facie* case of obviousness, and the burden has shifted to Appellant to rebut this showing.

Appellant nonetheless asserts that one skilled in the art would not "have any idea how to make a more lightly doped region over a more heavily doped region, as well as a more lightly doped region under the more heavily doped region" (Appeal Brief, at page 5, fourth paragraph); that "[doing so] is not so simple" (Appeal Brief, at page 6, line 3); and "[m]ore likely, [making all three n/n+/n layers] was too difficult a proposition for any of the cited references" (Appeal Brief, at page 6, second full paragraph). However, these assertions constitute bald conclusions and mere speculation, unsupported by facts or evidence. It is well settled that the arguments and mere allegations of Appellant's attorney do not constitute, nor substitute for, factual evidence.

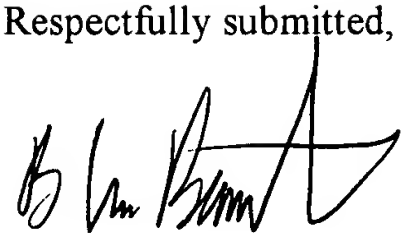
Appellant has not provided any references or affidavits explaining why forming both of the more lightly doped n regions together with the n+ region was any more difficult that forming only either one of these n-regions with the n+ region. In fact, Appellant has provided absolutely no evidence whatsoever that the formation of all three, n/n+/n layers produced *any* technological challenge to the reasonably skilled artisan. Appellant's only basis for asserting that the skilled artisan *was not able* to form all four diode layers in a bulk Si substrate, is the fact that none of

Ovshinsky, Chang or Slotboom actually did so. However, the fact that these three inventive entities either failed to consider providing, or chose to not provide, their diodes with all four layers, is *not* evidence that, given the motivation to do so, one of ordinary skill in the art would not have been *able* to provide these four layers solely in bulk Si.

To the contrary, Appellant's statements actually support the examiner's position that providing all four of the diode layers in the bulk substrate was a modification that was well within the reasonably skilled artisan's ability. Appellant states in the Summary of Invention section of the present appeal, "the exact nature of the ion-plantation [sic: ion-implantation] steps [for forming the diode] may be subject to considerable variation" (Appeal Brief, page 3, last paragraph). This statement evidences that there is nothing special, novel or inventive about how the diode's layers are formed, but rather that a wide array of conventional techniques may be employed.

In conclusion, the Appellant has **not** disputed the fact that combining the prior art in the manner set forth by the rejection would arrive at the present invention as claimed. Appellant has **not** disputed any of the motivations for combining the references. Appellant only asserts that the skilled artisan was not technologically able to combine the references in this manner. However, Appellant has provided absolutely no evidence that the ordinarily skilled artisan would have been unable to form all four diode layers solely in bulk silicon, much less provided the amount of evidence of this assertion that would be sufficient to rebut the examiner's *prima facie* case of obviousness. Because the examiner has made a *prima facie* showing of obviousness, the Appellant has failed to rebut this *prima facie* showing, and for the other reasons set forth above as well, it is believed that the rejections should be sustained.

Respectfully submitted,



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BRADLEY BAUMEISTER
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June 11, 2004

Conferees

Tom Thomas,
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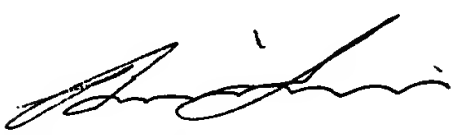

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